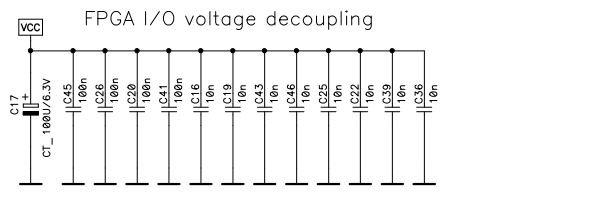
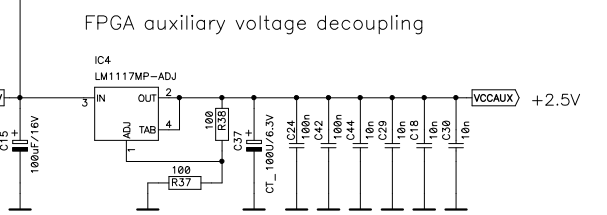
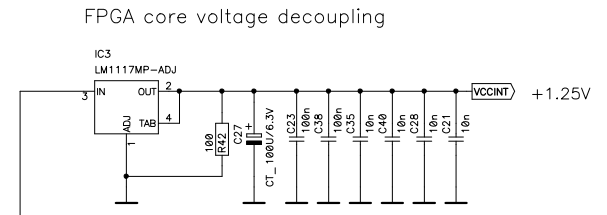
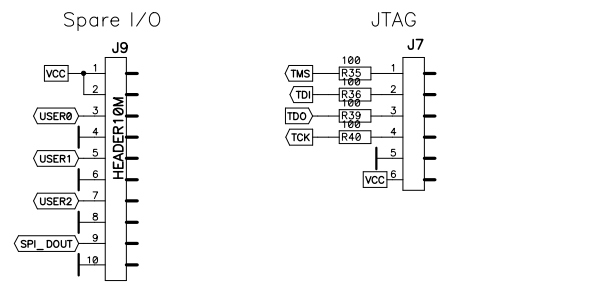
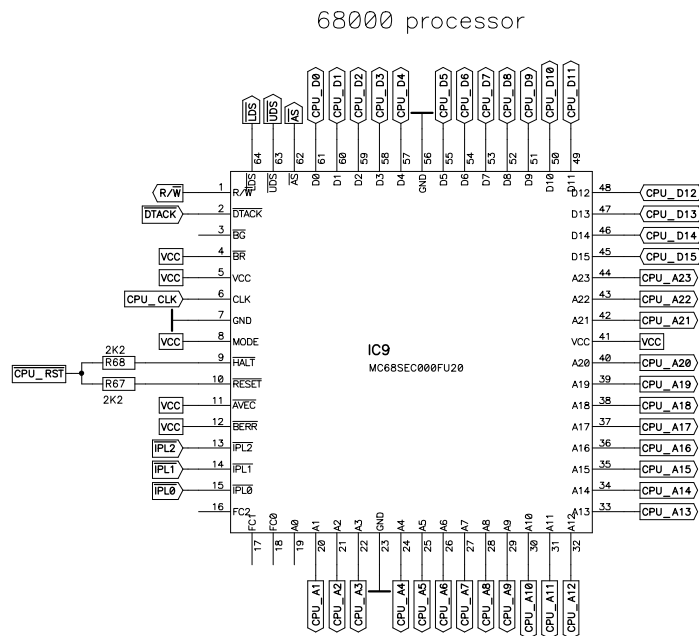


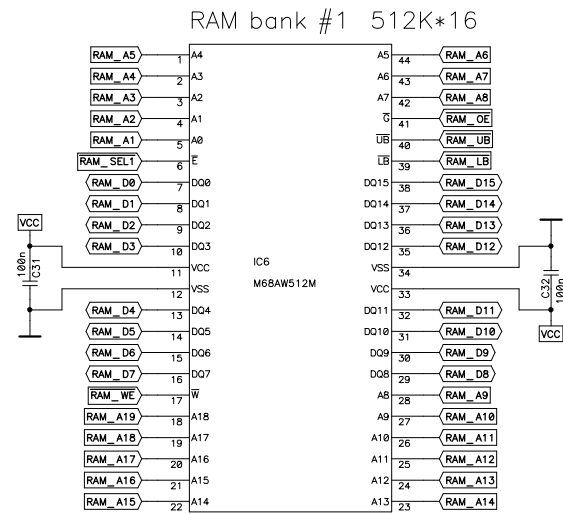
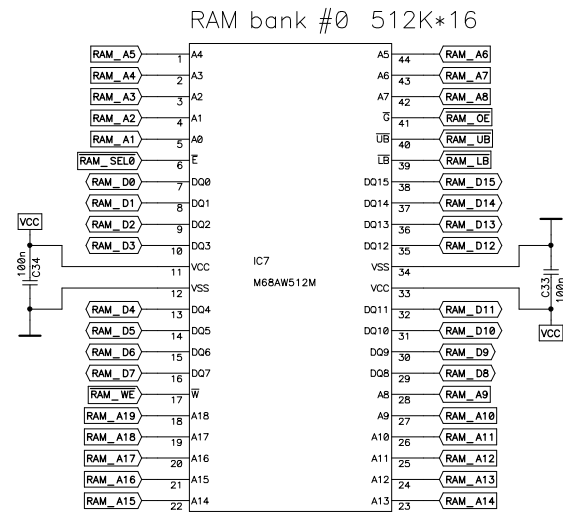
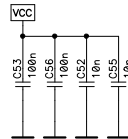
Changes from REV 1.0:  
 \* SPI\_DOUT is now connected to pin 19 of the FPGA  
 \* PS/2 connectors shielding is now connected to frame ground  
 \* R49 is now 100 Ohm  
 \* no more wire patches needed!



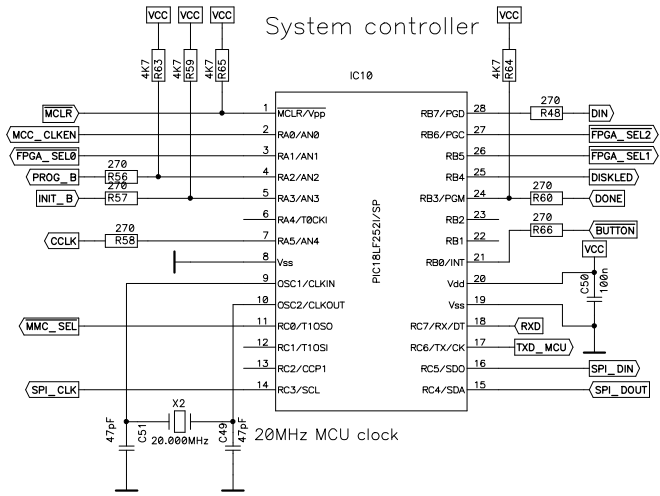
Title MINIMIG REV 1.1		
Size A2	Number SPARTAN POWER	Rev 2
Date 03-10-2007	Drawn by Dennis van Weeren	
Filename Minig11	Sheet 1	of 3



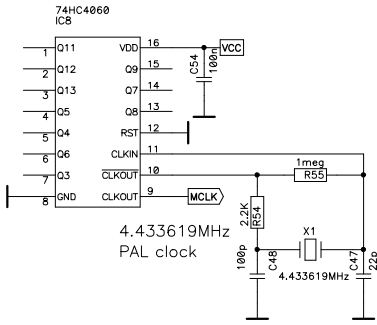
68000 decoupling



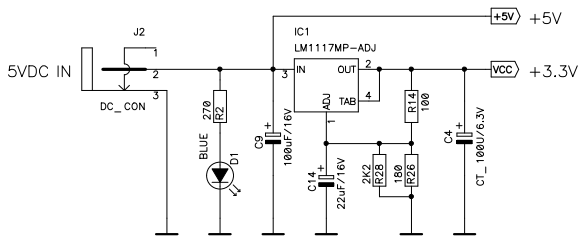
Title MINIMIG REV 1.1		
Size A2	Number 68000 FOREVER & RAM	Rev 2
Date 03-10-2007	Drawn by Dennis van Weeren	
Filename Minimig11	Sheet 2	of 3



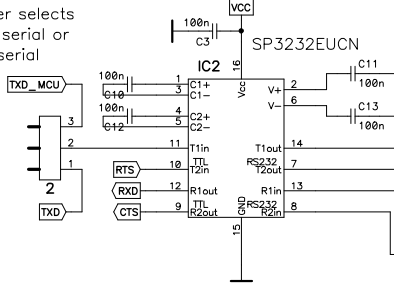
### Clock generator



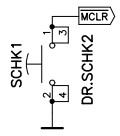
### Main power supply



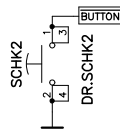
jumper selects  
FPGA serial or  
MCU serial



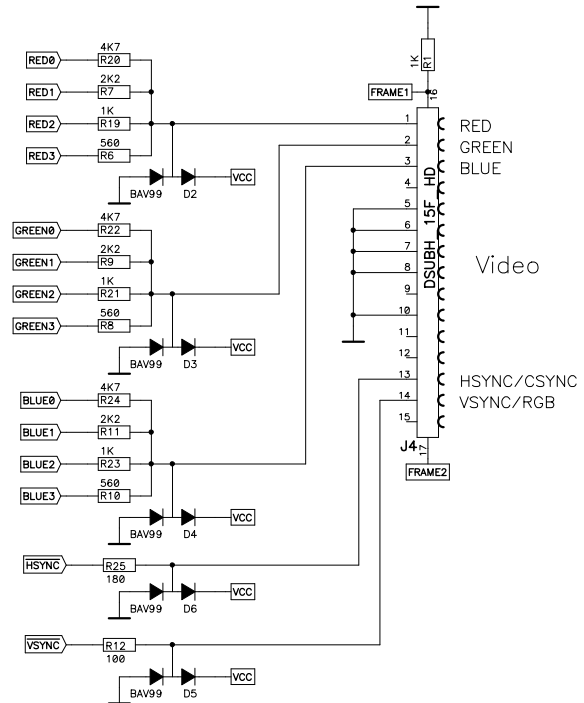
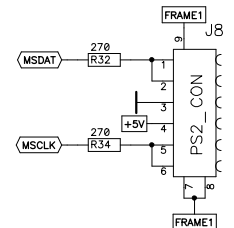
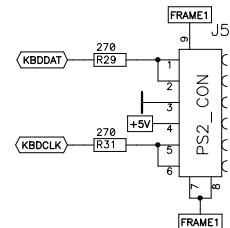
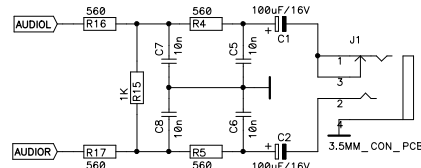
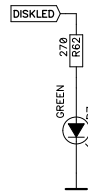
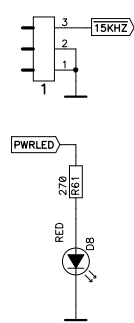
Programmers button



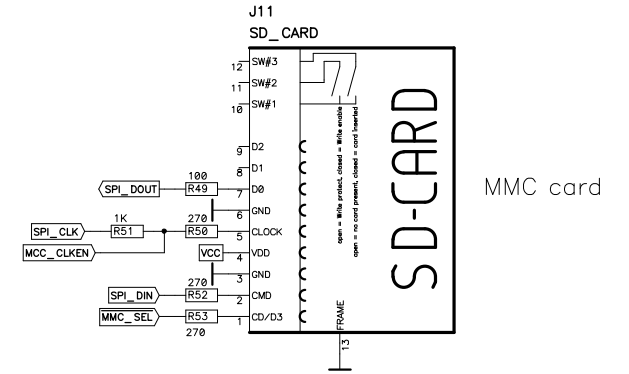
Button selects menu



jumper selects  
31KHz VGA mode or  
15KHz PAL mode



in 15kHz mode:  
VSYNC = high (scart RGB enable)  
HSYNC = composite sync



Title		
MINIMIG REV 1.1		
Size	Number	Rev
A2	I/O GALORE	2
Date	03-10-2007	Drawn by Dennis van Weeren
Filename	Minig11	Sheet 3 of 3